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PATENT
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAE-HO LEE

Serial No.:	10/774,608	Examiner:	*To be Assigned*
Filed:	10 February 2004	Art Unit:	2879

For: PLASMA DISPLAY PANEL AND METHOD OF MANUFACTURE THEREOF

INFORMATION DISCLOSURE STATEMENT

Mail Stop: Non-Fee Amendment
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes, and provides copies of the following art references:

U.S. PATENT REFERENCES:

- U.S. Patent No. RE37,444 to Kanazawa, entitled *METHOD AND APPARATUS FOR DRIVING DISPLAY PANEL*, reissued on 13 November 2001;
- U.S. Patent No. 5,541,618 to Shinoda, entitled *METHOD AND A CIRCUIT FOR GRADATIONALLY DRIVING A FLAT DISPLAY DEVICE*, issued on 30 July 1996;
- U.S. Patent No. 5,661,500 to Shinoda *et al.*, entitled *FULL COLOR SURFACE DISCHARGE TYPE PLASMA DISPLAY DEVICE*, issued on 26 August 1997;
- U.S. Patent No. 5,663,741 to Kanazawa, entitled *CONTROLLER OF PLASMA DISPLAY PANEL AND METHOD OF CONTROLLING THE SAME*, issued on 2 September 1997;
- U.S. Patent No. 5,674,553 to Sinoda *et al.*, entitled *FULL COLOR SURFACE DISCHARGE TYPE PLASMA DISPLAY DEVICE*, issued on 7 October 1997;

- U.S. Patent No. 5,724,054 to Shinoda, entitled *METHOD AND A CIRCUIT FOR GRADATIONALLY DRIVING A FLAT DISPLAY DEVICE*, issued on 3 March 1998;

- U.S. Patent No. 5,786,794 to Kishi *et al.*, entitled *DRIVER FOR FLAT DISPLAY PANEL*, issued on 28 July 1998;

- U.S. Patent No. 5,952,782 to Nanto *et al.*, entitled *SURFACE DISCHARGE PLASMA DISPLAY INCLUDING LIGHT SHIELDING FILM BETWEEN ADJACENT ELECTRODE PAIRS*, issued on 14 September 1999;

- U.S. Patent No. 6,630,916 to Shinoda, entitled *METHOD AND A CIRCUIT FOR GRADATIONALLY DRIVING A FLAT DISPLAY DEVICE*, issued on 7 October 2003; and

- U.S. Patent No. 6,707,436 to Setoguchi *et al.*, entitled *METHOD FOR DRIVING PLASMA DISPLAY PANEL*, issued on 16 March 2004.

FOREIGN PATENT REFERENCES:

- Japanese Patent Publication No. 01-325888 to Terao *et al.*, entitled *PLASMA DISPLAY AND ITS MANUFACTURING METHOD*, published 22 November 2001; and

- Japanese Patent Publication No. 01-043804 to Komatsu *et al.*, entitled *PLASMA DISPLAY AND MANUFACTURE THEREOF*, published 16 February 2001.

- Japanese Patent No. 2917279 issued on 23 April 1999, and the related Patent No. 2845183 issued on 30 October 1998, and Publication No. 02-148645 published on 7 June 1990, to Nanto *et al.*, entitled *GAS DISCHARGE PANEL*, together with an English language Abstract and translation of the specification.

OTHER DOCUMENTS:

- "*Final Draft International Standard*", Project No. 47C/61988-1/Ed.1; Plasma Display Panels - Part 1: Terminology and letter symbols, published by International Electrotechnical Commission, IEC. in 2003, and Appendix A - Description of Technology, Annex B - Relationship Between Voltage Terms And Discharge Characteristics; Annex C - Gaps and Annex D - Manufacturing.

DISCUSSION

Kanazawa U.S '444 relates to an apparatus and method for driving a display panel, e.g., an AC PDP, having a first substrate, at least one display line including first electrodes and second electrodes disposed in parallel with each other on the first substrate, a second substrate facing the first substrate, and third electrodes disposed on the second substrate and extending orthogonally to the first and second electrodes, in which write operations of the display data by light emission is executed by carrying out a selective write discharge utilizing a memory function, which as adapted to execute a write discharge for all cells and to execute an erase discharge for all cells before the selective write discharge, to thereby accumulate wall charges over the third electrodes in advance.

Shinoda U.S.'618 relates to a method and circuit of driving a flat display panel formed of a plurality of cells each having a memory function, where the cells are formed at cross points of a plurality of X-electrodes and a plurality of Y-electrode orthogonal to the X-electrodes, a period of a frame for displaying a single picture is divided into a plurality of sequential subframes. Each of the subframes has an addressing period during which cells to be lit later in a display period are selected from all the cells by being written by having a wall charge therein; and the display period subsequent to the address period for lighting the selected cells by applying sustain pulses to all the cells. A number of the sustain pulses included in each display period is predetermined differently for each subframe according to the weight given to each subframe. Gradation of visual brightness of each cell is determined by the accumulated number of the sustain pulses included in the subframes that are selectively operated during a single frame according to a required brightness level for each cell. Thus, an adequate time length is asserted to be allocated to required numbers of subframes to achieve a quality brightness-gradation for each cell.

Shinoda *et al.*U.S.'500 relates to a full color three electrode surface discharge type plasma display device that has fine image elements and is large and has a bright display. The three primary color luminescent areas are arranged in the extending direction of the display electrode pairs in a successive manner and an image element is composed by the three unit luminescent areas defined

by these three luminescent areas and address electrodes intersecting these three luminescent areas. Further, phosphors are coated not only on a substrate but also on the side walls of the barriers and on address electrodes. The manufacturing processes and operation methods of the these constructions are also disclosed.

Kanazawa U.S.'741 relates to a controller for a plasma display having a first drive unit to apply voltage to a sustain electrode of a display unit having a memory function and a second drive unit to apply voltage to an address electrode of the display unit. The first drive unit has a discharge control unit to control the discharge waveform of the voltage applied to the sustain electrode of the display unit. The discharge control unit has a delay element and a switching element connected in series between sustain electrodes. Alternatively, the control unit has a delay element and a switching element connected in series between the sustain electrodes and a constant voltage discrimination element connected in parallel with the delay element.

Shinoda *et al.*U.S.'553 relates to a full color three electrode surface discharge type plasma display device that has fine image elements and is large and has a bright display. The three primary color luminescent areas are arranged in the extending direction of the display electrode pairs in a successive manner and an image element is composed by the three unit luminescent areas defined by these three luminescent areas and address electrodes intersecting these three luminescent areas. Phosphors are coated not only on a substrate but also on the side walls of the barriers and on address electrodes. The manufacturing processes and operation methods of these constructions are also disclosed.

Shinoda U.S. '054 relates to a method and circuit for driving a flat display panel formed of a plurality of cells each having a memory function, where the cells are formed at cross points of a plurality of X-electrodes and a plurality of Y-electrode orthogonal to the X-electrodes, a period of a frame for displaying a single picture is divided into a plurality of sequential subframes. Each of the subframes has an addressing period during which cells to be lit later in a display period are selected

from all the cells by being written by having a wall charge therein; and the display period subsequent to the address period for lighting the selected cells by applying sustain pulses to all the cells. A number of the sustain pulses included in each display period is predetermined differently for each subframe according to the weight given to each subframe. Gradation of visual brightness of each cell is determined by the accumulated number of the sustain pulses included in the subframes that are selectively operated during a single frame according to a required brightness level for each cell. Thus, an adequate time length can be allocated to required numbers of subframes to achieve a quality brightness-gradation for each cell.

Kishi U.S.'794 relates to a flat panel display that has a low withstand voltage and performs high speed line sequential scanning and recovers power. An AC type panel display has electrodes arranged in a matrix form, a push-pull type driver circuit, having first and second transistors, provided for each pair of plural pairs, with power supply lines connected to a driver circuit for driving a plurality of display electrodes to be scanned and a power supply which supplies a defined voltage to one of the respective power supply lines of each pair connected to the corresponding driver circuit, and a leakage control switch which leaks the defined voltage applied to the power supply line.

Nanto *et al.*U.S.'782 relates to a surface discharge type plasma display panel(PDP) which includes a pair of front and rear substrates (11, 21) with a discharge space (30) therebetween and a plurality of pairs of display electrodes on an internal surface of either the front or rear substrate. The display electrodes extend along each display line L. The PDP further includes a light shielding film (45), having a belt shape extending along the display line direction, formed on either internal or outer surface of the front substrate (11) to overlap each area S2 between the adjacent display lines L and is sandwiched between the display electrodes X and Y.

Shinoda U.S. '916 relates to a method and circuit of driving a flat display panel formed of a plurality of cells each having a memory function, wherein the cells are formed at cross points of

a plurality of X-electrodes and a plurality of Y-electrodes orthogonal to the X-electrodes, and a period of a frame for displaying a single picture is divided into a plurality of sequential subframes. Each of the subframes has an address period, during which cells to be lit later in a display period are selected from among all of the cells by being written so as to have a wall charge therein, and a display period, subsequent to the address period, for lighting the selected cells by applying sustain pulses to all the cells. A number of sustain pulses included in each display period is predetermined differently for each subframe, according to a weight given to each subframe. Gradation of visual brightness of each cell is determined by the accumulated number of the sustain pulses included in the subframes that are selectively operated during a single frame according to a required brightness level for each cell. An adequate time accumulation is thereby allocated to a required number of subframes to achieve a quality brightness-gradation for each cell.

Setoguchi *et al.*U.S.'436 discloses a method for driving a plasma display panel in which a plurality of first electrodes and second electrodes are arranged parallel to each other, a plurality of third electrodes are arranged to cross the first and second electrodes, and discharge cells are defined with areas in which the electrodes cross mutually are arranged in the form of a matrix. According to the driving method, a reset period is a period during which the distribution of wall charges in the plurality of discharge cells is uniformed. An addressing period is a period during which wall charges are produced in the discharge cells according to display data. A sustain discharge period is a period during which a sustained discharge is induced in the discharge cells in which wall charges are produced during the addressing period. The driving method in accordance with the present invention has a step of applying a first pulse in which an applied voltage varies with time so as to induce a first discharge in the lines defined by the first and second electrodes, and a step of applying a second pulse in which an applied voltage varies with time so as to induce a second discharge as erase an discharge in the lines defined by the first and second electrodes. These steps are carried out during the reset period.

Terao *et al.* JP' 888 relates a plasma display, with each of partition walls 15 arranged

integrally on a substrate glass 12, where partition walls 17 for arranging electrodes are arranged therebetween. An electrode 18 and a dielectric layer 19 are provided on each upper edge thereof. The manufacturing method uses steps of forming of wall where each partition wall 15 is formed integrally on the substrate glass 12; forming of the partition walls for arranging electrodes where the partition walls 17 for arranging the electrodes are provided between the partition walls 15; forming electrodes where each electrode 18 is provided on the upper edge of the partition wall 17 for arranging the electrode; and forming of dielectric layer where the dielectric layer 19 is provided on each electrode 18.

Komatsu *et al.* JP' 804 relates to a pattern 12P which is formed by photoresist 12R on substrate glass 12A, and substrate glass 12A in a part the pattern 12P is cut by sandblast to form a partition wall 18. After a process for cutting the substrate glass 12A and forming the partition wall 18, a process for forming an electrode 16 on the substrate glass 12 and a process for forming a phosphor 19 within a discharge cell 17 are performed and the partition wall 18 is constituted integrally with the substrate glass 12.

Nanto *et al.*, JP' 279, JP' 645, and JP' 183 (which is a divisional of Nanto *et al.* '279), together with an English language Abstract and translation of the specification, all relate to an electrode support base 11 which is formed of a transparent glass base, and mutually adjacent discharge keeping electrodes of each pair of transparent discharge keeping electrodes on the base, for example, between 321 and 312, are short circuited by a thick metal material layer 33 such as gold Au. When a voltage pulse is applied to the electrode drawing metal material layer 33, the discharge also simultaneously occurs in a read discharge cell related to the adjacent non-selected keeping discharge cell to which the voltage pulse is applied. By the discharge of the selected keeping discharge cell, a phosphor 23 provided on a cover base 21 generates an excited color display light and directly exhibits a color display on the display observing surface of the transparent electrode support base 11, to permit an observer to visually recognize a highly bright and clear color display.

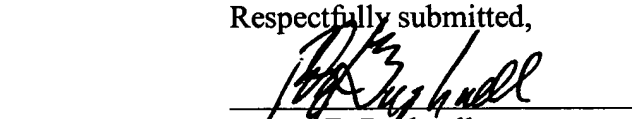
The "***Final Draft International Standard***", Project No. 47C/61988-1/Ed.1, presents a list of nomenclature and a corresponding explanation of the nomenclature, together with waveform components, and Appendix A - Description of Technology; Annex B - Relationship Between Voltage Terms And Discharge Characteristics; Annex C - Gaps and Annex D - Manufacturing; collectively describe and graphically illustrate the principles of operation and manufacture for plasma display panels (PDP's) contemporary to the industry.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

Copies of U.S. Patents and U.S. Patent Application Publications cited in this Information Disclosure Statement are not provided herewith, in accordance with U.S. Patent & Trademark Office OG Notice dated 5 August 2003 stating that the requirement under 37 CFR 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication is waived for all U.S. national patent applications filed after 30 June 2003. A copy of the U.S. Patent & Trademark Office OG Notice dated 5 August 2003 is attached to this Information Disclosure Statement.

No fee is incurred by this Statement.

Respectfully submitted,



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	APPLICANT TAE-HO LEE	
	FILING DATE 10 February 2004	GROUP 2879

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	RE37,444	11/01	*Kanazawa*			
	5,541,618	07/96	*Shinoda*			
	5,661,500	08/97	*Shinoda et al.*			
	5,663,741	09/97	*Kanazawa*			
	5,674,553	10/97	*Sinoda et al.*			
	5,724,054	03/98	*Shinoda*			
	5,786,794	07/98	*Kishi et al.*			
	5,952,782	09/99	*Nanto*			
	6,630,916	10/03	*Shinoda*			
	6,707,436	03/04	*Setoguchi et al.*			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLAS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	JP 2001-325888	11/01	JAPAN			Abstract	
	JP 2001-043804	02/01	JAPAN			Abstract	
	JP 2917279	04/99	JAPAN			Abstract	
	JP 02-148645	06/90					
	JP 2845183	10/98					

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

	"*Final Draft International Standard*", Project No. 47C/61988-1/Ed.1; Plasma Display Panels - Part 1: Terminology and letter symbols, published by International Electrotechnical Commission, IEC. in 2003, and Appendix A - Description of Technology, Annex B - Relationship Between Voltage Terms And Discharge Characteristics; Annex C - Gaps and Annex D - Manufacturing

EXAMINER:	DATE CONSIDERED:

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

United States Patent and Trademark Office OG Notices: 05 August 2003

Information Disclosure Statements May Be Filed Without Copies of U.S. Patents and Published Applications in Patent Applications filed after June 30, 2003

Background

The U.S. Patent and Trademark Office (USPTO or Office) regulations concerning Information Disclosure Statements (IDSs) currently require that copies of the cited references be submitted with the IDS listing. See 37 CFR 1.98 (a)(2). In a prior notice in the Official Gazette this requirement was partially waived with respect to U.S. patents and U.S. patent application publications when an applicant submitted an IDS using the Office's electronic filing system (as an electronic IDS, eIDS). See Legal Framework for the Use of the Electronic Filing System, 1263 Off. Gaz. Pat. Off. 60, 10/8/2002, Part V.

All U.S. applications1 filed after June 30, 2003 are stored in electronic form in the Office's Image File Wrapper (IFW) system.2 IDSs submitted for these electronic applications are processed by Office staff to create an electronic link which permits cited U.S. patents and U.S. patent application publications to be conveniently viewed by examiners through the Office's patent search system. This feature enables the Office to avoid scanning these documents into IFW, obviating the need for their submission.

Waiver

The Office hereby waives the requirement under 37 CFR 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC 371 after June 30, 2003. See 37 CFR 1.491(b). For all patent applications filed on or before June 30, 2003, copies of cited U.S. patents and patent application publications are still required unless an eIDS is filed.

Applicants are still required to submit copies of foreign patent documents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

FOR FURTHER INFORMATION CONTACT:

Questions concerning this waiver may be submitted to Jay Lucas by e-mail at Jay.Lucas@uspto.gov or by telephone at (703) 308-6868. Comments may also be submitted by mail addressed to: Commissioner for Patents, Box Comments - Patents, Post Office Box 1450, Alexandria, VA 22313-1450, or by facsimile to (703) 305-2919, marked to the attention of Jay Lucas.

STEPHEN G. KUNIN
Deputy Commissioner for
Patent Examination Policy

1 Except in special situations, such as in applications under secrecy order or containing national security markings.

2 See Notification of United States Patent and Trademark Office Patent Application Records being Stored and Processed in Electronic Form, 1271 Off. Gaz. Pat. Off. 100, 6/17 2003.